

EXHIBIT 014

U.S. Patent No. 7,373,449 (Radulescu and Goossens)
“Apparatus and method for communicating in an integrated circuit”

'449 Patent Claim	Samsung Product Including Exynos System on Chip ¹
10. Method for exchanging messages in an integrated circuit comprising a plurality of modules,	<p>Without conceding that the preamble of claim 10 of the '449 Patent is limiting, the Samsung Galaxy A53 (hereinafter, the “Samsung product”) performs a method for exchanging messages in an integrated circuit comprising a plurality of modules, either literally or under the doctrine of equivalents.</p> <p>The Samsung product includes an integrated circuit. For example, the Samsung product includes the Exynos 1280 system on chip (hereinafter, the “Exynos SoC”).</p>  <p>Samsung Galaxy A53 Exynos 1280 https://semiconductor.samsung.com/processor/showcase/smartphone/</p>

¹ The Samsung product is charted as a representative product made used, sold, offered for sale, and/or imported by Samsung. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

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	<p>The Exynos SoC comprises a plurality of modules, for example Arm Cortex-A78 core, Cortex-A55 core, Arm Mali-G68 GPU, and AI Engine with NPU:</p> <h2 style="font-size: 1.5em; font-weight: bold; margin-bottom: 0;">Specifications</h2> <hr/> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #4f81bd; color: white;"> <th colspan="2" style="text-align: center; padding: 5px;">Exynos 1280</th> </tr> </thead> <tbody> <tr> <td style="padding: 5px;">CPU</td><td style="padding: 5px;">Cortex®-A78 x 2 + Cortex®-A55 x 6</td></tr> <tr> <td style="padding: 5px;">GPU</td><td style="padding: 5px;">Mali™-G68</td></tr> <tr> <td style="padding: 5px;">AI</td><td style="padding: 5px;">AI Engine with NPU</td></tr> <tr> <td style="padding: 5px;">Modem</td><td style="padding: 5px;">5G NR Sub-6GHz 2.55Gbps (DL) / 1.28Gbps (UL) 5G NR mmWave 1.84Gbps (DL) / 0.92Gbps (UL) LTE Cat.18 6CC 1.2Gbps (DL) / Cat.18 2CC 200Mbps (UL)</td></tr> <tr> <td style="padding: 5px;">Connectivity</td><td style="padding: 5px;">WiFi 802.11ac MIMO with Dual-band (2.4/5G), Bluetooth® 5.2, FM Radio Rx</td></tr> <tr> <td style="padding: 5px;">GNSS</td><td style="padding: 5px;">Quad-constellation multi-signal for L1 and L5 GNSS</td></tr> <tr> <td style="padding: 5px;">Camera</td><td style="padding: 5px;">Up to 108MP in single camera mode, Single-camera 32MP @30fps</td></tr> <tr> <td style="padding: 5px;">Video</td><td style="padding: 5px;">4K 30fps encoding and decoding</td></tr> <tr> <td style="padding: 5px;">Display</td><td style="padding: 5px;">Full HD+@120Hz</td></tr> <tr> <td style="padding: 5px;">Memory</td><td style="padding: 5px;">LPDDR4x</td></tr> <tr> <td style="padding: 5px;">Storage</td><td style="padding: 5px;">UFS v2.2</td></tr> <tr> <td style="padding: 5px;">Process</td><td style="padding: 5px;">5nm</td></tr> </tbody> </table> <p style="margin-top: 10px;">https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf</p> <p>The Exynos SoC included in the Samsung product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) to exchange messages:</p>	Exynos 1280		CPU	Cortex®-A78 x 2 + Cortex®-A55 x 6	GPU	Mali™-G68	AI	AI Engine with NPU	Modem	5G NR Sub-6GHz 2.55Gbps (DL) / 1.28Gbps (UL) 5G NR mmWave 1.84Gbps (DL) / 0.92Gbps (UL) LTE Cat.18 6CC 1.2Gbps (DL) / Cat.18 2CC 200Mbps (UL)	Connectivity	WiFi 802.11ac MIMO with Dual-band (2.4/5G), Bluetooth® 5.2, FM Radio Rx	GNSS	Quad-constellation multi-signal for L1 and L5 GNSS	Camera	Up to 108MP in single camera mode, Single-camera 32MP @30fps	Video	4K 30fps encoding and decoding	Display	Full HD+@120Hz	Memory	LPDDR4x	Storage	UFS v2.2	Process	5nm
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	<p>Samsung</p>  <p>Samsung uses Arteris FlexNoC IP in its Samsung Exynos mobile phone applications processors, digital baseband modems, 4K SUHD TVs and Artik IoT modules.</p> <p>LEARN MORE »</p> <p>https://web.archive.org/web/20210514110614/https://www.arteris.com/customers</p>

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	<p>Arteris IP FlexNoC® Interconnect Licensed by Samsung's System LSI Business for Digital TV Chips</p> <p>by Kurt Shuler, on April 23, 2019</p> <p>CAMPBELL, Calif. –April 23, 2019– Arteris IP, the world's leading supplier of innovative, silicon-proven network-on-chip (NoC) interconnect semiconductor intellectual property, today announced that Samsung's System LSI Business has renewed multiple Arteris IP FlexNoC Interconnect licenses for use in multiple high-performance digital TV (DTV) processing chips utilizing Samsung's latest semiconductor technology process nodes.</p> <p>“Over many years, FlexNoC interconnect IP has helped us accelerate implementation of our digital TV chip designs on our latest semiconductor process nodes. This core interconnect technology is required to develop complex and highly optimized chips in a predictable, low-risk fashion.”</p> <p style="text-align: center;">SAMSUNG</p> <p><i>Jaeyoul Lee, Vice President, Samsung Electronics</i></p> <p>Samsung first licensed FlexNoC Interconnect IP in 2010. Since then, Samsung has used Arteris interconnect IP to enable complex SoC architectures in chips like the Exynos mobile processors and other electronic systems.</p> <p>https://www.arteris.com/press-releases/samsung-lsi-dtv-arteris-ip-flexnoc</p>

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	<p>Arteris Interconnect IP Solution Selected by Samsung for Mobile SoC Deployment</p> <p>by Kurt Shuler, on November 02, 2010</p> <p>Network-on-Chip (NoC) interconnect technology leader enables higher performance and more cost effective designs for mobile phone systems-on-chip (SoCs)</p> <p>SUNNYVALE, California — November 2, 2010 — Arteris, Inc., a leading supplier of on-chip interconnect IP solutions, today announced that Samsung Electronics Co., Ltd., has selected Arteris' interconnect solutions for multiple chips within Samsung's mobile SOC products. Samsung chose Arteris interconnect IP to support the high speed inter-chip communication requirements in next generation mobile SOC products.</p> <p>“The Arteris interconnect IP offers us a convenient solution to handle the high speed communication needed between our SoC and external modem IC. Our customers will benefit from the lower BOM cost and power consumption as a result of this IP. We look forward to Arteris' interconnect IP helping us shorten development schedules and lower risks associated with compatibility.</p> <p>The Samsung logo is a blue oval containing the word "SAMSUNG" in white capital letters.</p> <p><small>Thomas Kim, Vice President, SoC Platform Development, System LSI, Samsung Electronics</small></p> <p>https://www.arteris.com/press-releases/pr_2010_nov_02?hsLang=en-us</p>

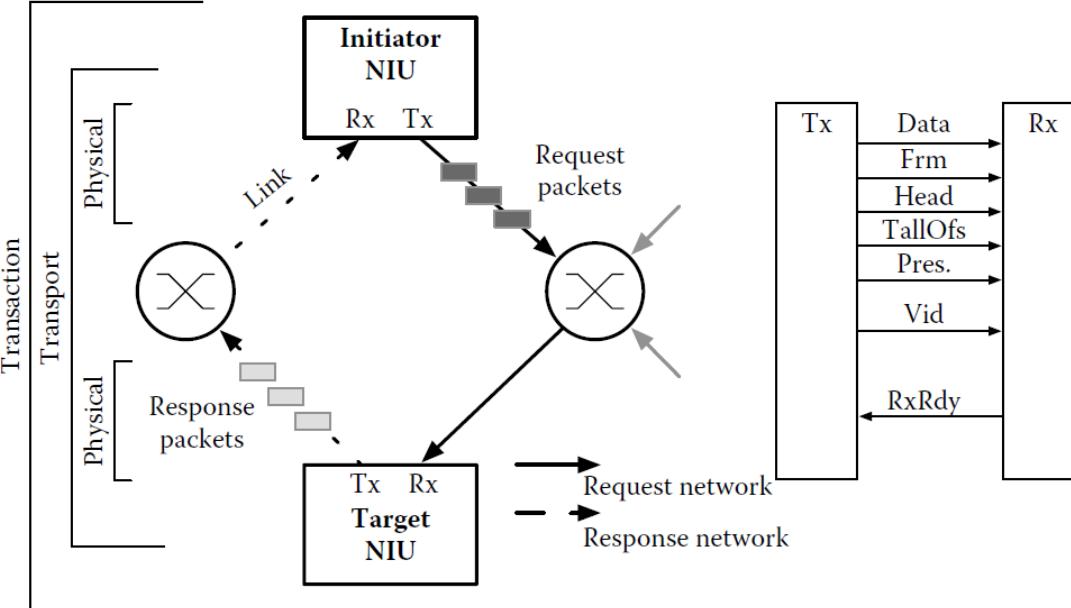
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	<p>The Arteris NoC exchanges messages in the Exynos SoC included in the Samsung product.</p> <p>For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p style="text-align: center;"><i>11.3.1.1 Transaction Layer</i></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

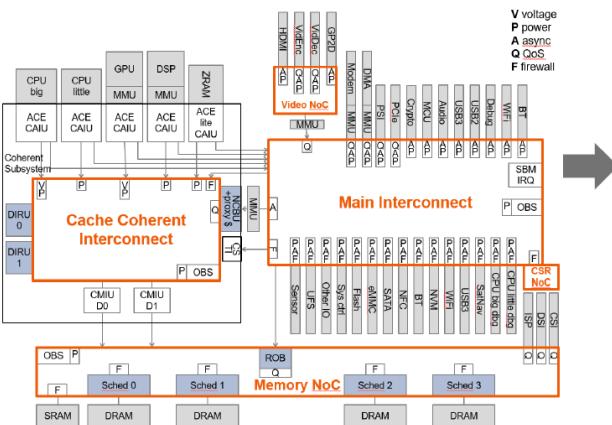
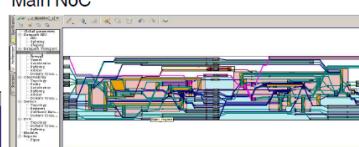
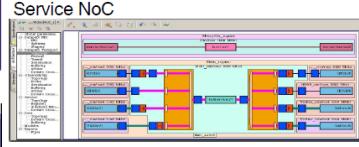
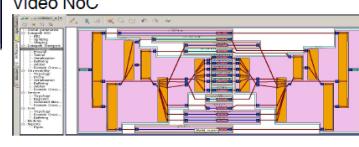
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	<p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”).</p>
the messages between the modules being	Without conceding that the preamble of claim 10 of the '449 Patent is limiting, the Arteris NoC exchanges messages between modules in the Exynos SoC included in the Samsung product over connections via a network, wherein said connections comprises a set of communication channels

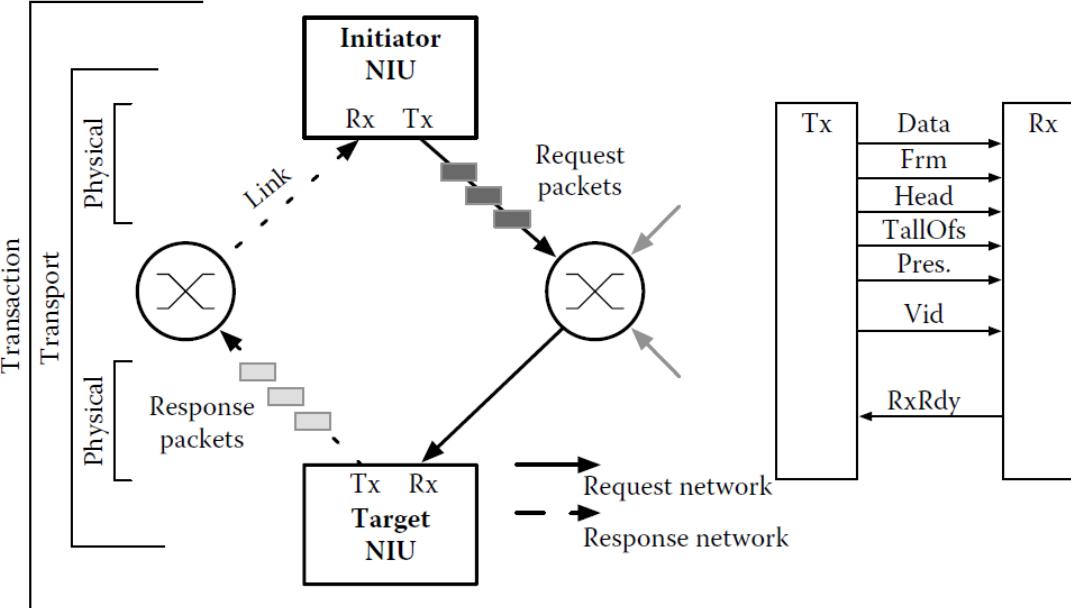
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<p>exchanged over connections via a network, wherein said connections comprises a set of communication channels each having a set of connection properties, any communication channel being independently configurable,</p>	<p>each having a set of connection properties any communication channel being independently configurable, either literally or under the doctrine of equivalents.</p> <p>A large SoC, such as the Exynos SoC included in the Samsung product may include multiple classes of Arteris NoC interconnect network:</p> <p style="text-align: center;">Logical Interconnect Topology Development</p> <p style="text-align: center;">FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</p>  <p>The diagram illustrates the logical interconnect topology development for a system-on-chip. It shows the Main Interconnect connecting various IP blocks such as CPU big, CPU little, GPU, DSP, MMU, and DRAM. The interconnect is divided into several NoC classes: Cache Coherent, Video, Main, Memory, and CSB. The Cache Coherent NoC connects Coherent Subsystems (DIRU 0, DIRU 1) and CMU D0/D1. The Main Interconnect connects to various functional blocks like GPU, DSP, MMU, and DRAM. The Memory NoC connects SRAM and DRAM. The CSB NoC connects Sched 0-3. The Video NoC connects various video-related blocks. A legend defines symbols: V voltage, P power, A async, Q QoS, and F firewall.</p> <p style="text-align: right;"> Main NoC  Service NoC  Memory NoC  Video NoC  </p> <ul style="list-style-type: none"> • ArChip16 Example: Large SoCs have multiple classes of interconnect <ul style="list-style-type: none"> – Non-coherent, Coherent, Control/Status, Observability, etc. • Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.</p>

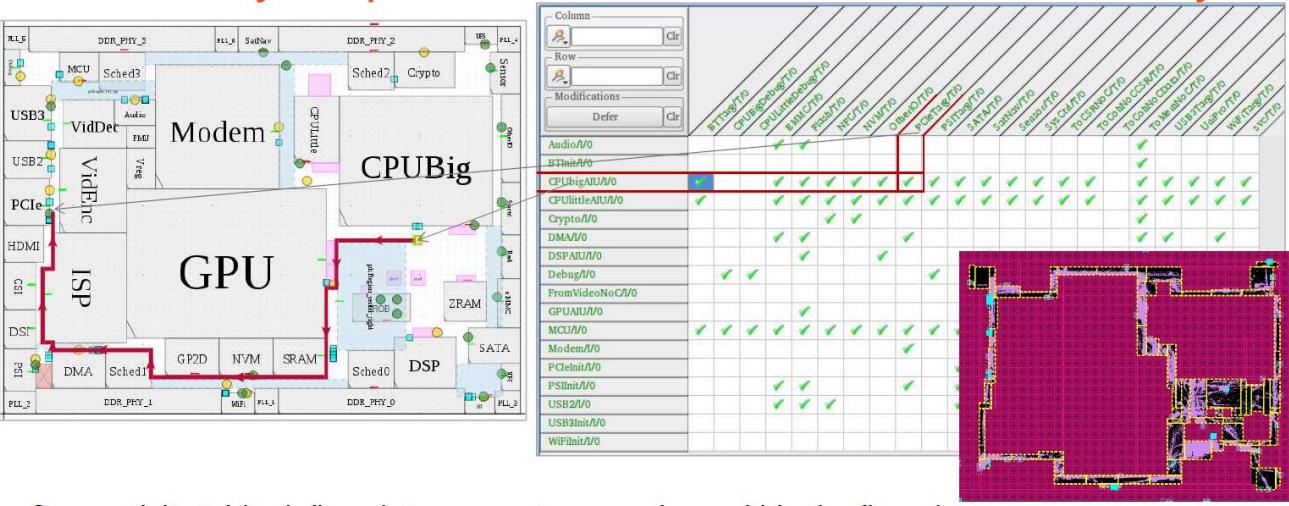
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	<p>The Exynos SoC included in the Samsung product utilizes the Arteris NoC to exchange messages over connections via a network, wherein said connections comprises a set of communication channels that are independently configurable.</p> <p>For example, in the the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p> <p>Connections within the Arteris NoC network may be defined by a connectivity table:</p>

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	<p style="text-align: center;">Connectivity Map → Interconnect Connections → Layout</p>  <ul style="list-style-type: none"> • Connectivity table defines interconnect connections within the floorplan • Routes must pass through available channels in the floorplan • Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU <p style="text-align: right;">DC-Topographical</p> <div style="display: flex; justify-content: space-between;"> ARTERIS IP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 12 </div> <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.</p> <p>In the Arteris NoC, “[t]he delivery of packets within the NoC is the responsibility of the physical layer [where the] link size, or width (i.e., number of wires), is set by the designer at design time[and] [o]ne link (represented in Figure 11.1) defines the following signals... Pres.—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2) [and] RxRdy—flow control”:</p>

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	<p>11.3.1.3 Physical Layer</p> <p>The delivery of packets within the NoC is the responsibility of the physical layer. Packets, which have been split by the transport layer into cells, are delivered as words that are sent along links. Within a single clock cycle, the physical layer may carry words comprising a fraction of a cell, a single cell, or multiple cells. The link size, or width (i.e., number of wires), is set by the designer at design time and determines the number of cells of one word. NTTP defines five possible link-widths: quarter (QRT), half (HLF), single (SGL), double (DBL), and quad (QUAD). A single-width (SGL) link transmits one cell per clock cycle, a double-width link transmits two cells per clock cycle, and so on. Words travel within point-to-point links, which are independent from other protocol layers: a word is sent through a transmit port, Tx, over a link to a receive port, Rx. The actual number of wires in a link depends on the</p>

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	<p>maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals:</p> <ul style="list-style-type: none">• Data—Data word of the width specified at design-time.• Frm—When asserted high, indicates that a packet is being transmitted.• Head—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only.• TailOfs—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only.• Pres.—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2).• Vld—Data valid: when asserted high, indicates that a word is being transmitted.• RxRdy—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. <p>This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.</p>
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	<p><i>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313-314.</i></p> <p>The Exynos SoC included in the Samsung product utilizes the Arteris NoC's connections that comprise a set of communication channels each having a set of connection properties, any communication channel being independently configurable.</p> <p>For example, as noted above, in the Arteris NoC, “[o]ne link (represented in Figure 11.1) defines the following signals... Pres.—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service) [and] RxRdy—flow control.”</p> <p>In the Arteris NoC implements Quality of Service (QoS) to “provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic”:</p> <p>Quality of Service (QoS). The QoS is a very important feature in the inter-connect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in Æthereal NoC [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT.</p> <p>In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure</p>

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	<p>signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair.</p> <p>The Arteris NoC supports the following four different traffic classes:</p>

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	<ul style="list-style-type: none"> ● Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. ● Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. ● Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. ● Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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	<p>* Note that in the NTTP packet, the pressure field allows more than one bit, resulting in multiple levels of preferred traffic.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 315-316.</p> <p>As a further illustration, the Arteris NoC “addresses … varied QoS needs in many ways,” including “Dynamic Packet Priorities” and “Dynamic Pressure Propagation”:</p> <h2 style="text-align: center;">Arbitration: Dynamic Packet Priorities & Dynamic Pressure Propagation</h2> <p>Arteris Network on Chip technology addresses these varied QoS needs in many ways: First, the interconnect assigns priorities to transactions to ensure they arrive at the target in the proper order to meet system requirements. Priority levels can be attached to individual packets or to all transactions pending on a socket. The interconnect can also assign Dynamic Packet Priorities at runtime.</p> <p>Second, the interconnect can sense when high priority packets may be blocked or slowed due to downstream traffic congestion and can then clear a path for these high priority packets. This technology, called Dynamic Pressure Propagation, is analogous to a fire truck racing down city streets: All traffic pulls to the side of the road to let the fire truck through.</p> <p>https://www.arteris.com/end-to-end-quality-of-service-qos</p>

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	<p>As a further illustration, “QoS information may be generated from within the [Arteris] NoC interconnect using Arteris’ QoS Generator”:</p> <h2 data-bbox="523 421 1486 486">Bandwidth Limiters and Rate Regulators</h2> <p>Many times architects will want to implement QoS within their SoC but the QoS prioritization data is not available from the individual IP blocks. In this case, QoS information may be generated from within the NoC interconnect using Arteris’ QoS Generator. The QoS Generator can instantiate sophisticated, and software programmable, means to regulate interconnect QoS, including:</p> <ul style="list-style-type: none"> <li data-bbox="578 845 1649 975">> Bandwidth Limiters – Bandwidth limiters cause a socket to stop accepting requests when a run-time programmable throughput threshold has been exceeded. <li data-bbox="578 985 1712 1165">> Rate Regulators – Rate regulators cause a socket’s transactions to be demoted when a bandwidth threshold is reached. This can be considered a smoother version of the bandwidth limiter because transactions are only demoted instead of stalled. <p data-bbox="508 1192 1368 1225">https://www.arteris.com/end-to-end-quality-of-service-qos</p> <p>As a further illustration, the Arteris NoC uses “a mechanism called rated adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.” For other traffic, the “[b]est effort traffic can be left untouched[,]” “[l]atency sensitive traffic may have its</p>

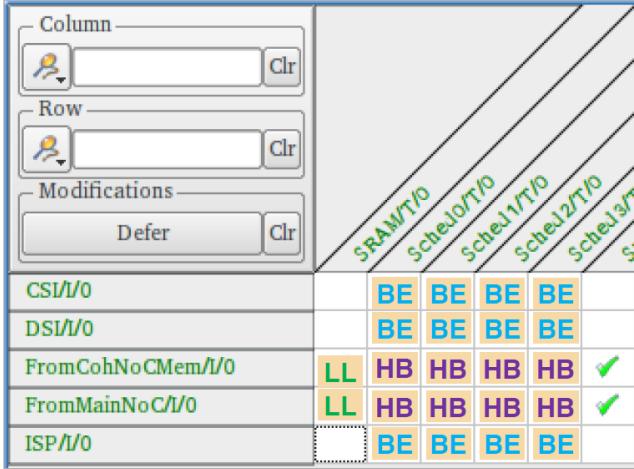
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	<p>urgency modulated as a function of the transaction[,]” “[s]oft real-time traffic may have its hurry level modulated as a function of the bandwidth it receives[,]” and “[o]n the real-time modem data port, the hurry is fixed at a critical level”:</p> <p>Those effects can be mended by the insertion of buffering. In the case of peak bandwidth reduction, a simple FIFO does the job: Busy states present at the output of the FIFO do not propagate back to the input until the FIFO is full. For a peak bandwidth increase, the situation is a bit more complex. In a FIFO, wait states present at the input are only absorbed when the FIFO is not empty. Arteris proposes a mechanism called rate adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.</p> <p>In this second step, the architecture is modified to introduce some buffering. In our example 760 bytes of memory have been distributed across the topology. Some have been put on existing links; some required the creation of new links.</p> <p>See Application driven network-on-chip architecture exploration & refinement for a complex SoC, https://www.arteris.com/hs-fs/hub/48858/file-14363521-pdf/docs/springerappdrivennocarchitecture8.5x11.pdf, at pg.16.</p> <p>For the other traffic, “the configuration can be done in architecture”:</p>

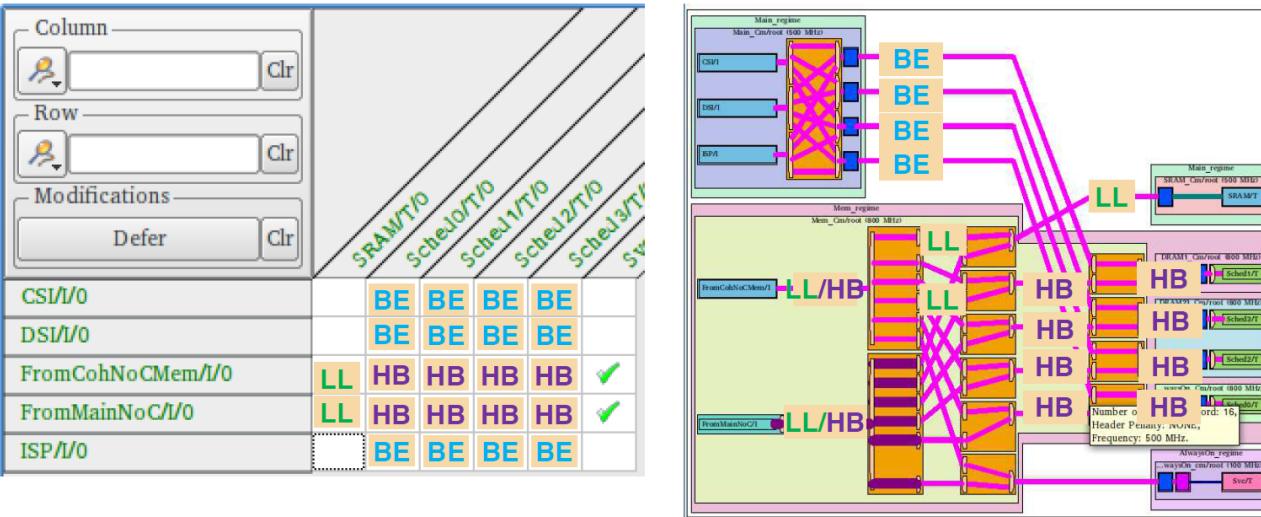
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	<ul style="list-style-type: none"> ● Best effort traffic can be left untouched. ● Latency sensitive traffic may have its urgency modulated as a function of the transaction: <i>Normal</i> for writes and <i>important</i> for reads. ● Soft real-time traffic may have its hurry level modulated as a function of the bandwidth it receives: <i>Critical</i> until a specified bandwidth is obtained on a sliding 4 microsecond window, and <i>normal</i> thereafter. These settings are set through configuration registers and may be modified while the interconnect is running. The mechanism is called a bandwidth regulator. ● On the real-time modem data port, the hurry is fixed at a critical level. <p><i>Id.</i> at 18.</p> <p>As a further illustration, connections within the Arteris NoC may be classified by traffic class and traffic classes may be mapped onto the Arteris interconnect topology:</p>

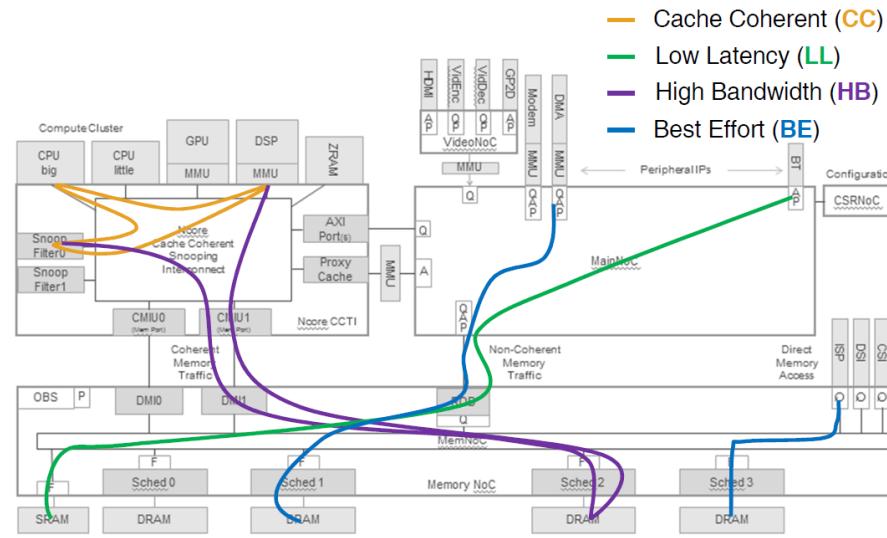
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	<p>Memory NoC: Interconnect Topology – Traffic Classes</p> <p>Classify your IP connections per class of traffic:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Best Effort (BE)</td> <td>Image system</td> </tr> <tr> <td>Low Latency (LL)</td> <td>SRAM</td> </tr> <tr> <td>High Bandwidth (HB)</td> <td>Main/Coherency</td> </tr> </table> 	Best Effort (BE)	Image system	Low Latency (LL)	SRAM	High Bandwidth (HB)	Main/Coherency
Best Effort (BE)	Image system						
Low Latency (LL)	SRAM						
High Bandwidth (HB)	Main/Coherency						

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	<p>Memory NoC: Traffic classes are mapped onto logical interconnect topology</p>  <p>Table: Mapping of I/O Types to Traffic Classes</p> <table border="1"> <tr> <td>Column</td> <td>SRAM/T/0</td> <td>Sched0/T/0</td> <td>Sched1/T/0</td> <td>Sched2/T/0</td> <td>Sched3/T/0</td> <td>Sched4/T/0</td> </tr> <tr> <td>Row</td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> </tr> <tr> <td>Modifications</td> <td>Defer</td> <td>Clr</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>CSI/I/O</td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td></td> <td></td> </tr> <tr> <td>DSI/I/O</td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td></td> <td></td> </tr> <tr> <td>FromCohNoCMem/I/O</td> <td>LL</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>✓</td> </tr> <tr> <td>FromMainNoC/I/O</td> <td>LL</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>✓</td> </tr> <tr> <td>ISP/I/O</td> <td></td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td></td> </tr> </table>	Column	SRAM/T/0	Sched0/T/0	Sched1/T/0	Sched2/T/0	Sched3/T/0	Sched4/T/0	Row	BE	BE	BE	BE	BE	BE	Modifications	Defer	Clr					CSI/I/O	BE	BE	BE	BE			DSI/I/O	BE	BE	BE	BE			FromCohNoCMem/I/O	LL	HB	HB	HB	HB	✓	FromMainNoC/I/O	LL	HB	HB	HB	HB	✓	ISP/I/O		BE	BE	BE	BE	
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FromMainNoC/I/O	LL	HB	HB	HB	HB	✓																																																			
ISP/I/O		BE	BE	BE	BE																																																				

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	<h2 style="color: red; text-align: center;">Memory Access Traffic Classes</h2>  <ul style="list-style-type: none"> • Cache Coherent (CC) within Compute Cluster • Low Latency (LL) to SRAM • High Bandwidth (HB) to DRAM & Cache Fill • Best Effort (BE) for Peripherals & DMA • QoS for Video • Multiple functional NoCs interacting • Physically Constrained <p style="text-align: center;"><small>ARTERIS IP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 11</small></p> <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slides 11, 13, 16.</p> <p>As a further illustration, in the Arteris NoC, “QoS is supported in the switch using pressure information generated by the IP itself and embedded in NTTP packets” and “[s]ome features [of the switch] can be software-controlled at runtime through the service network”:</p>

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	<p><i>11.3.3.1 Switching</i></p> <p>The switching is done by accepting NTTP packets carried by input ports and forwarding each packet transparently to a specific output port. The switch is characterized with a fully synchronous operation and can be implemented as a full crossbar (up to one data word transfer per port and per cycle), although there is an automatic removal of hardware corresponding to unused input/output port connections (port depletion). The switch uses wormhole routing, for reduced latency, and can provide full throughput arbitration; that is, up to one routing decision per input port and per cycle. An arbitrary number of switches can be connected in cascade, supporting any loopless network topology. The QoS is supported in the switch using the pressure information generated by the IP itself and embedded in NTTP packets.</p> <p>A switch can be configured to meet specific application requirements by setting the MINI-ports (Rx or Tx ports, as defined by the MINI interface introduced earlier) attributes, routing tables, arbitration mode, and pipelining strategy. Some of the features can be software-controlled at runtime through</p>

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	<p>the service network. There is one routing table per Rx port and one arbiter per Tx port. Packet switching consists of the following four stages:</p> <ol style="list-style-type: none"> 1. Choosing the route—Using relevant information extracted from the packet, the routing table selects a target output port. 2. Arbitrating—Because more than a single input port can request a given output port at a given time, an arbiter selects one requesting input port per output port. The arbiter maintains input/output connection until the packet completes its transit in the switch. 3. Switching—Once routing and arbitration decisions have been made, the switch transports each word of the packet from its input port to its output port. The switch implementation employs a full crossbar, ensuring that the switch does not contribute to congestion. 4. Arbiter release—Once the last word of a packet has been pipelined into the crossbar, the arbiter releases the output, making it available for other packets that may be waiting at other input ports. <p>The simplified block diagram of the switch architecture is shown in Figure 11.6.</p>

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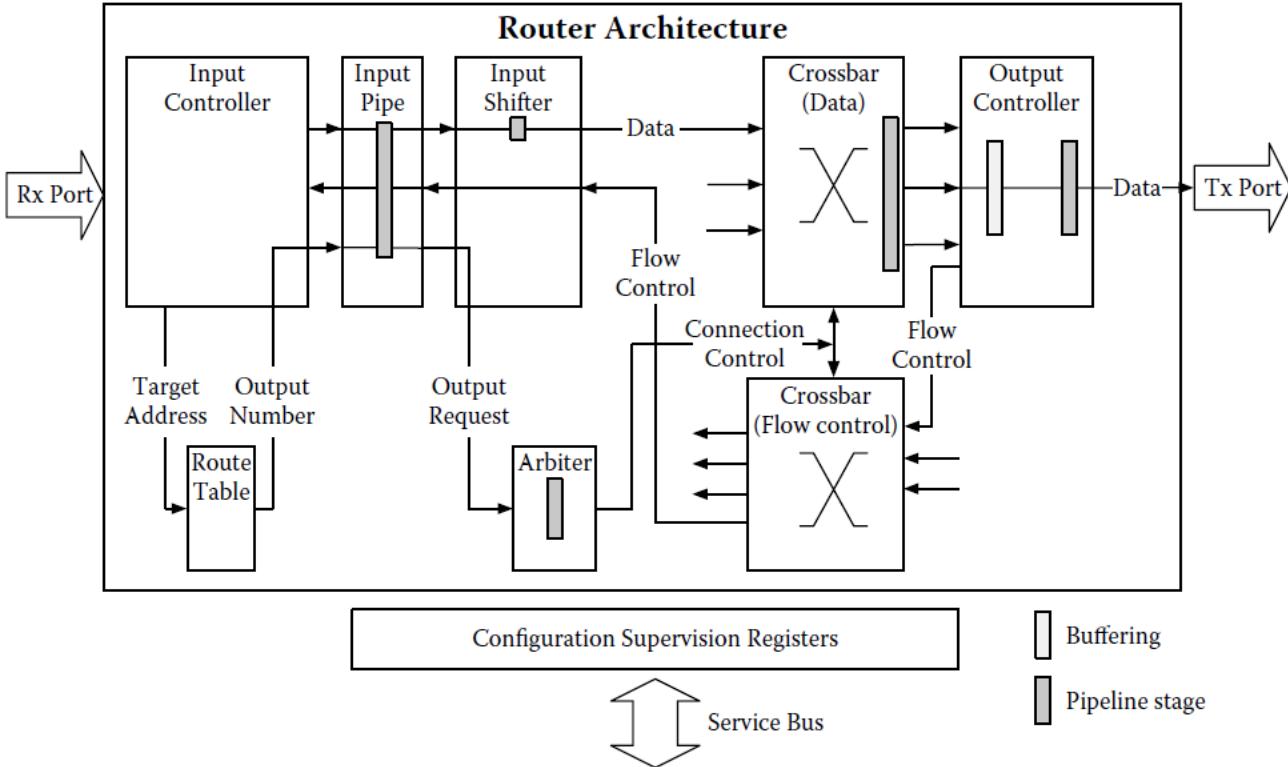
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	 <p>Router Architecture</p> <p>The diagram illustrates the Router Architecture. Data flows from the Rx Port through the Input Controller, Input Pipe, and Input Shifter to the Crossbar (Data). The Crossbar (Data) connects to the Output Controller, which then leads to the Tx Port. Control signals include Target Address, Output Number, and Route Table from the Input Controller; Output Request from the Input Shifter; Flow Control and Connection Control between the Crossbars; and a Service Bus connected to Configuration Supervision Registers.</p> <p>Legend:</p> <ul style="list-style-type: none"> Buffering (represented by a rectangle with a vertical line) Pipeline stage (represented by a rectangle with a diagonal line)

FIGURE 11.6
 Packet transportation unit: Router architecture.

See Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 319-320.

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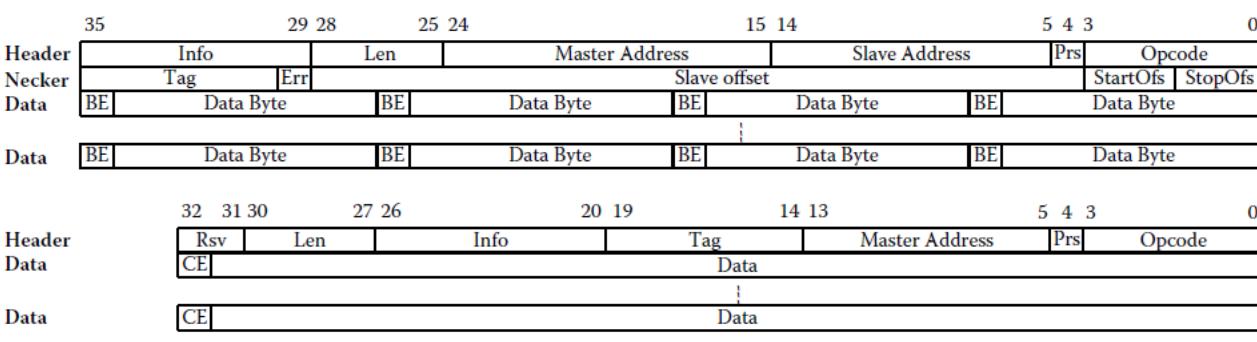
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	<p>As a further illustration, the “Pres.” signal in the NTTP packet “[i]ndicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2).”</p>  <p>The diagram illustrates the NTTP packet structure with two header formats and a data payload.</p> <p>Header: 35 bits total. Fields include Info (29-28), Len (25-24), Master Address (25-14), Slave Address (15-14), Prs (Priority), and Opcode (5-4, 3, 0).</p> <p>Necker: 35 bits total. Fields include Tag (31-30), Err (30-29), Slave offset (25-14), and StartOfs/StopOfs (5-4, 3, 0).</p> <p>Data: Data Byte fields (BE) for Header, Necker, and Data sections.</p> <p>Header: 32 bits total. Fields include Rsv (31-30), Len (27-26), Info (25-19), Tag (20-19), Master Address (14-13), Prs (Priority), and Opcode (5-4, 3, 0).</p> <p>Data: Data fields (CE) for Header and Data sections.</p>

FIGURE 11.2
NTTP packet structure.

See id. at 313, 314.

As a further illustration, in the Arteris NoC, “the routing tables actually used in the switch are parameterizable for each input port of the switch. It is thus possible to use different routing tables for each switch input. Routing tables can optionally be programmed via the service network interface; in this case, their configuration registers appear in the switch register address map.”

See id. at 322.

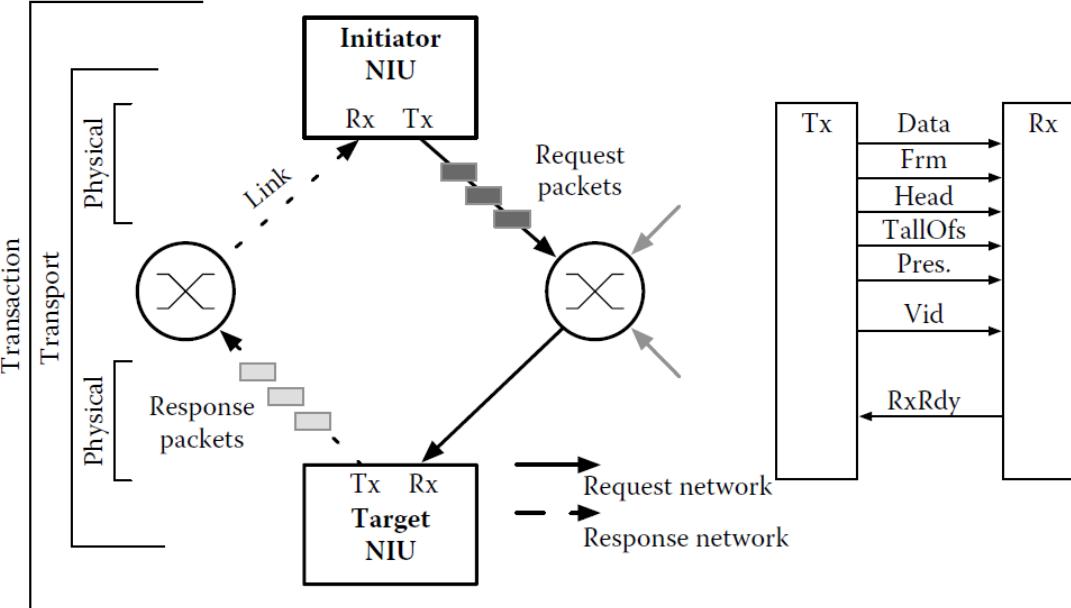
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<p>wherein said connection through the network supports transactions comprising at least one of outgoing messages from the first module to the second module and return messages from the second module to the first module</p>	<p>Without conceding that the preamble of claim 10 of the '449 Patent is limiting, the Arteris NoC in the Exynos SoC included in the Samsung product has connections through the network that support transactions comprising at least one of outgoing messages from the first module to the second module and return messages from the second module to the first module, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by the Exynos SoC included in the Samsung product, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p style="text-align: center;">11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p>
and further comprising the steps of: the first module issuing a request	In the Arteris NoC in the Exynos SoC included in the Samsung product, the first module issues a request for a connection with the second module to a communication manager, wherein the request comprises desired connection properties associated with the sets of communication channels, either literally or under the doctrine of equivalents.

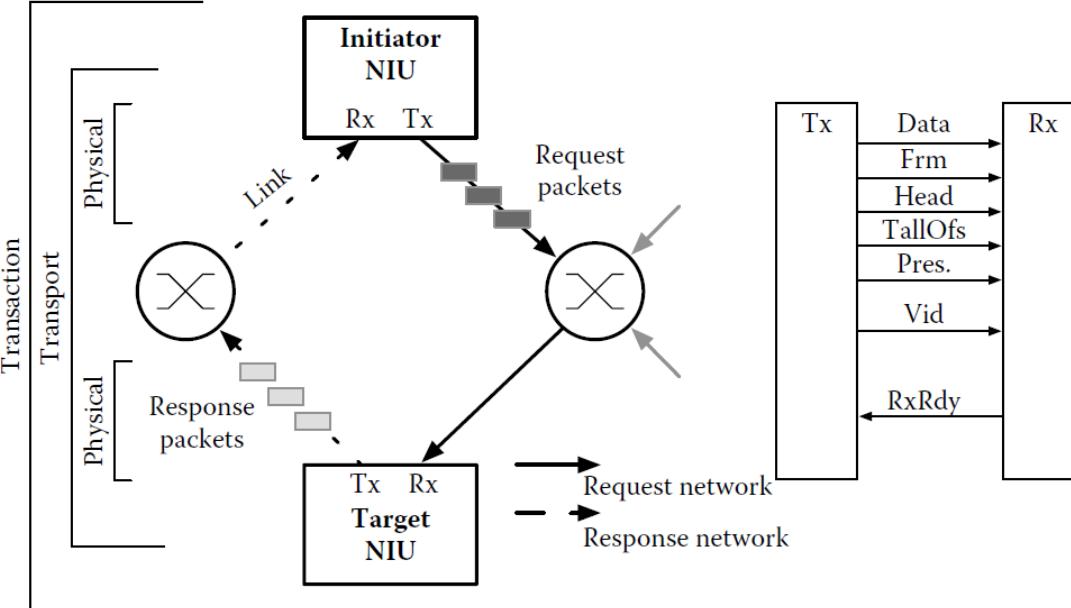
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<p>for a connection with the second module to a communication manager, wherein the request comprises desired connection properties associated with the sets of communication channels;</p>	<p>The first module of the Exynos SoC included in the Samsung product utilizes the Arteris NoC to issue a request for a connection with the second module to a communication manager.</p> <p>For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p style="text-align: center;">11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p> <p>The request issued by first module of the Exynos SoC included in the Samsung product comprises desired connection properties associated with the sets of communication channels.</p> <p>For example, in the Arteris NoC, “[t]he delivery of packets within the NoC is the responsibility of the physical layer [where the] link size, or width (i.e., number of wires), is set by the designer at design time[and] [o]ne link (represented in Figure 11.1) defines the following signals... Pres.—</p>

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	<p>Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2) [and] RxRdy – flow control”:</p> <p>11.3.1.3 Physical Layer</p> <p>The delivery of packets within the NoC is the responsibility of the physical layer. Packets, which have been split by the transport layer into cells, are delivered as words that are sent along links. Within a single clock cycle, the physical layer may carry words comprising a fraction of a cell, a single cell, or multiple cells. The link size, or width (i.e., number of wires), is set by the designer at design time and determines the number of cells of one word. NTTP defines five possible link-widths: quarter (QRT), half (HLF), single (SGL), double (DBL), and quad (QUAD). A single-width (SGL) link transmits one cell per clock cycle, a double-width link transmits two cells per clock cycle, and so on. Words travel within point-to-point links, which are independent from other protocol layers: a word is sent through a transmit port, Tx, over a link to a receive port, Rx. The actual number of wires in a link depends on the</p>

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	<p>maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals:</p> <ul style="list-style-type: none">• Data—Data word of the width specified at design-time.• Frm—When asserted high, indicates that a packet is being transmitted.• Head—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only.• TailOfs—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only.• Pres.—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2).• Vld—Data valid: when asserted high, indicates that a word is being transmitted.• RxRdy—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. <p>This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.</p>
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	<p><i>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313-314.</i></p> <p>As a further example, in the Arteris NoC, “QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition” where the “pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed” and the “pressure information will be embedded in the NTTP packet at the NIU level”:</p> <p>Quality of Service (QoS). The QoS is a very important feature in the inter-connect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in Æthereal NoC [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT.</p> <p>In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure</p>

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	<p>signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair.</p> <p>The Arteris NoC supports the following four different traffic classes:</p>

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	<ul style="list-style-type: none"> ● Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. ● Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. ● Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. ● Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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	<p>* Note that in the NTTP packet, the pressure field allows more than one bit, resulting in multiple levels of preferred traffic.</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;"></td> <td style="width: 15%; text-align: right;">35</td> <td style="width: 15%; text-align: right;">29 28</td> <td style="width: 15%; text-align: right;">25 24</td> <td style="width: 15%; text-align: right;">15 14</td> <td style="width: 15%; text-align: right;">5 4 3</td> <td style="width: 10%; text-align: right;">0</td> </tr> <tr> <td style="vertical-align: top;">Header</td> <td>Info</td> <td>Len</td> <td>Master Address</td> <td>Slave Address</td> <td>Prs</td> <td>Opcode</td> </tr> <tr> <td style="vertical-align: top;">Necker</td> <td>Tag</td> <td>Err</td> <td></td> <td>Slave offset</td> <td></td> <td>StartOfs StopOfs</td> </tr> <tr> <td style="vertical-align: top;">Data</td> <td>BE</td> <td>BE</td> <td>Data Byte</td> <td>BE</td> <td>Data Byte</td> <td>BE</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td style="vertical-align: top;">Data</td> <td>BE</td> <td>BE</td> <td>Data Byte</td> <td>BE</td> <td>Data Byte</td> <td>BE</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td style="vertical-align: top;">Header</td> <td>32 31 30</td> <td>27 26</td> <td>20 19</td> <td>14 13</td> <td>5 4 3</td> <td>0</td> </tr> <tr> <td style="vertical-align: top;">Data</td> <td>Rsv</td> <td>Len</td> <td>Info</td> <td>Tag</td> <td>Master Address</td> <td>Prs</td> </tr> <tr> <td></td> <td>CE</td> <td></td> <td></td> <td>Data</td> <td></td> <td>Opcode</td> </tr> <tr> <td style="vertical-align: top;">Data</td> <td>CE</td> <td></td> <td></td> <td>Data</td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table> <p>FIGURE 11.2 NTTP packet structure.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 315-316.</p> <p>As a further example, in the Arteris NoC, “QoS is supported in the switch using pressure information generated by the IP itself and embedded in NTTP packets” and the router architecture includes blocks such as “Input Controller,” “Flow Control,” “Crossbar (Flow control)” “Route Table” and “Arbiter”:</p>		35	29 28	25 24	15 14	5 4 3	0	Header	Info	Len	Master Address	Slave Address	Prs	Opcode	Necker	Tag	Err		Slave offset		StartOfs StopOfs	Data	BE	BE	Data Byte	BE	Data Byte	BE								Data	BE	BE	Data Byte	BE	Data Byte	BE															Header	32 31 30	27 26	20 19	14 13	5 4 3	0	Data	Rsv	Len	Info	Tag	Master Address	Prs		CE			Data		Opcode	Data	CE			Data									
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U.S. Patent No. 7,373,449 (Radulescu and Goossens)
“Apparatus and method for communicating in an integrated circuit”

'449 Patent Claim	Samsung Product Including Exynos System on Chip ¹
	<p><i>11.3.3.1 Switching</i></p> <p>The switching is done by accepting NTTP packets carried by input ports and forwarding each packet transparently to a specific output port. The switch is characterized with a fully synchronous operation and can be implemented as a full crossbar (up to one data word transfer per port and per cycle), although there is an automatic removal of hardware corresponding to unused input/output port connections (port depletion). The switch uses wormhole routing, for reduced latency, and can provide full throughput arbitration; that is, up to one routing decision per input port and per cycle. An arbitrary number of switches can be connected in cascade, supporting any loopless network topology. The QoS is supported in the switch using the pressure information generated by the IP itself and embedded in NTTP packets.</p> <p>A switch can be configured to meet specific application requirements by setting the MINI-ports (Rx or Tx ports, as defined by the MINI interface introduced earlier) attributes, routing tables, arbitration mode, and pipelining strategy. Some of the features can be software-controlled at runtime through</p>

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	<p>the service network. There is one routing table per Rx port and one arbiter per Tx port. Packet switching consists of the following four stages:</p> <ol style="list-style-type: none"> 1. Choosing the route—Using relevant information extracted from the packet, the routing table selects a target output port. 2. Arbitrating—Because more than a single input port can request a given output port at a given time, an arbiter selects one requesting input port per output port. The arbiter maintains input/output connection until the packet completes its transit in the switch. 3. Switching—Once routing and arbitration decisions have been made, the switch transports each word of the packet from its input port to its output port. The switch implementation employs a full crossbar, ensuring that the switch does not contribute to congestion. 4. Arbiter release—Once the last word of a packet has been pipelined into the crossbar, the arbiter releases the output, making it available for other packets that may be waiting at other input ports. <p>The simplified block diagram of the switch architecture is shown in Figure 11.6.</p>

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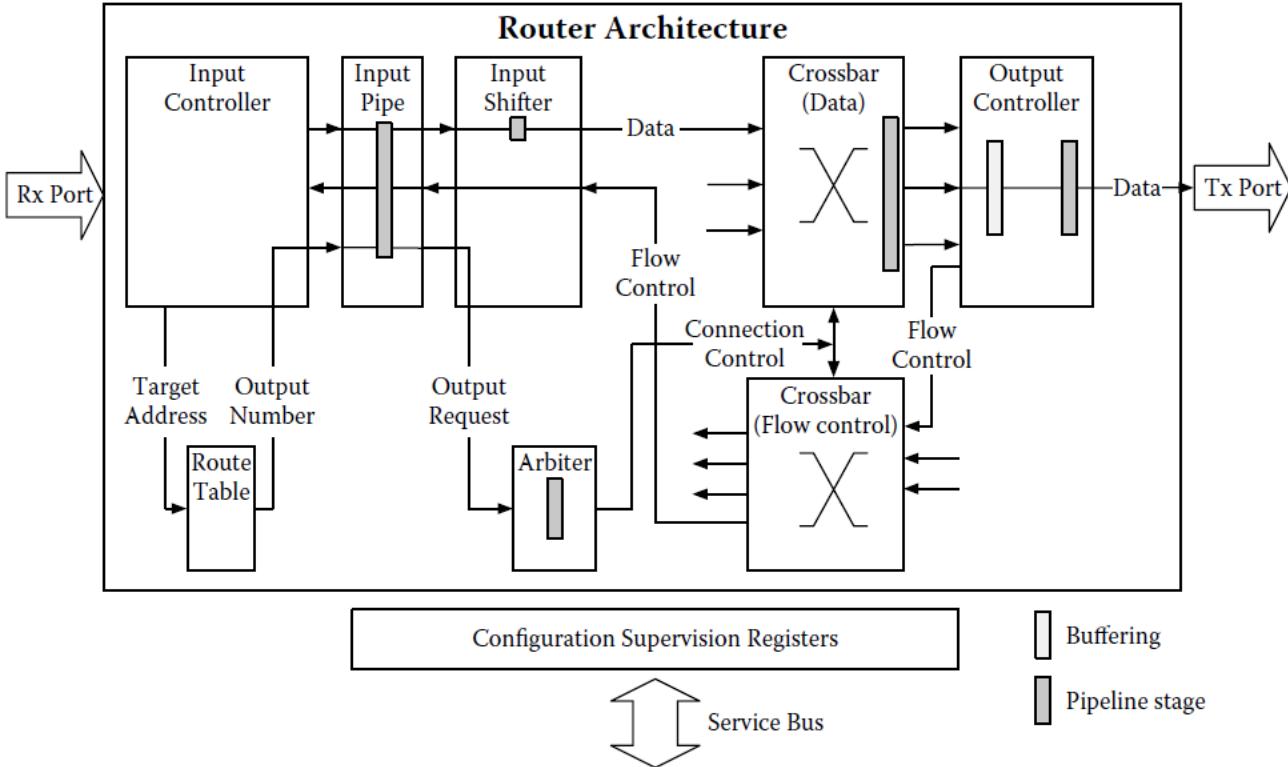
'449 Patent Claim	Samsung Product Including Exynos System on Chip ¹
	 <p>Router Architecture</p> <p>The diagram illustrates the Router Architecture of a Samsung Product Including Exynos System on Chip. The architecture is organized into several functional blocks:</p> <ul style="list-style-type: none"> Input Path: Data enters via the Rx Port and passes through the Input Controller, Input Pipe, and Input Shifter. Control Path: The Input Controller receives the Target Address and Output Number from the Route Table. It also receives an Output Request from the Arbiter. Switching and Buffering: The Input Shifter and Crossbar (Data) handle the data path. The Crossbar (Data) is controlled by Flow Control signals. Output Path: The output of the Crossbar (Data) is processed by the Output Controller and then sent to the Tx Port. Control Logic: The Arbiter manages the Output Request. The Connection Control unit manages connections between the Crossbar (Data) and Crossbar (Flow control). Both crossbars have Flow Control inputs. Configuration and Supervision: A Service Bus connects the Configuration Supervision Registers to the various components. Buffering: Pipeline stages are indicated by gray vertical bars at various points in the data path.

FIGURE 11.6

Packet transportation unit: Router architecture.

See Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 319-320.

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<p>the communication manager forwarding the request to a resource manager; the resource manager determining whether a target connection with the desired connection properties is available;</p>	<p>In the Arteris NoC in the Exynos SoC included in the Samsung product, the communication manager forwards the request to a resource manager and the resource manager determines whether a target connection with the desired connection properties is available, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by Exynos SoC included in the Samsung product, “QoS is supported in the switch” which “choos[es] the route” using a “routing table”; “arbitrat[es]”; and “switch[es]” and the router architecture includes blocks such as “Input Controller,” “Flow Control,” “Crossbar (Flow control)” “Route Table” and “Arbiter”:</p>

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FIGURE 11.6

Packet transportation unit: Router architecture.

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	<p>As a further illustration, in the Arteris NoC, “the pressure information used to define the preferred traffic class (QoS) of the requesting inputs... [t]he pressure information is given top priority by the switch arbiter” and “the input controller extracts pertinent data from packet headers, forwards it to the routing table, fetches back the target output number, and then sends a request to the arbiter. After arbitration is granted, the input controller transmits the rest of the packet to the crossbar. The request to the arbiter is sustained as long as the last word of the packet has not been transferred. Upon transferring the last cell of the packet, the arbiter is allowed to select a new input.”</p> <p><i>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 321, 322.</i></p>
the resource manager responding with the availability of the target connection to the communication manager; and	<p>In the Arteris NoC in the Exynos SoC included in the Samsung product, the resource manager responds with the availability of the target connection to the communication manager, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by the Exynos SoC included in the Samsung product, “the pressure information used to define the preferred traffic class (QoS) of the requesting inputs... [t]he pressure information is given top priority by the switch arbiter” and “the input controller extracts pertinent data from packet headers, forwards it to the routing table, fetches back the target output number, and then sends a request to the arbiter. After arbitration is granted, the input controller transmits the rest of the packet to the crossbar. The request to the arbiter is sustained as long as the last word of the packet has not been transferred. Upon transferring the last cell of the packet, the arbiter is allowed to select a new input.”</p> <p><i>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 321, 322.</i></p>

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the target connection between the first and second module being established based on the available properties of said communication channels of said connection.	<p>In the Arteris NoC in the Exynos SoC included in the Samsung product, the target connection between the first and second module is established based on the available properties of said communication channels of said connection, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by the Exynos SoC included in the Samsung product, “QoS is supported in the switch” which “choos[es] the route” using a “routing table”; “arbitrat[es]”; and “switch[es]”:</p>

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FIGURE 11.6

Packet transportation unit: Router architecture.

See Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 319-320.

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